

The SP5055 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I<sup>2</sup>C BUS format. The device contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I<sup>2</sup>C BUS. The device has one fixed I<sup>2</sup>C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

### FEATURES

- Complete 2.6GHz Single Chip System
- Programmable via I<sup>2</sup>C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi-Directional
- 5 Level ADC
- Variable I<sup>2</sup>C BUS Address For Multi Tuner Applications
- Full ESD Protection\*

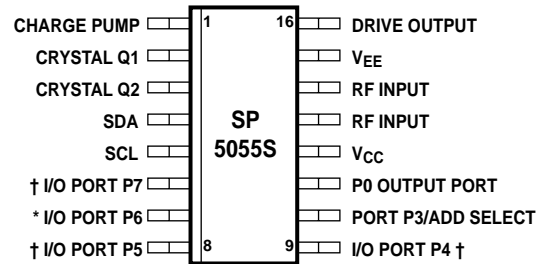
\* Normal ESD handling procedures should be observed.

DS2361

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**Ordering Information**  
 SP5055GS/KG/MPAS (Tubes)  
 SP5055GS/KG/MPAD (Tape & Reel)  
 16lead miniature plastic package



† = Logic level I/O  
 \* = 3-bit ADC input

**MP16**

Fig. 1 Pin connections – top view

### APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

## ELECTRICAL CHARACTERISTICS

$T_{amb} = -20^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$ ,  $V_{CC} = +4.7\text{V}$  to  $5.3\text{V}$ .

These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Reference frequency = 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		65	80	mA	$V_{CC} = 5\text{V}$
Prescaler input voltage	13, 14	50		300	mV <sub>RMS</sub>	500MHz to 2.6GHz Sinewave
Prescaler input voltage	13, 14	100		300	mV <sub>RMS</sub>	120MHz, see Fig. 5
Prescaler input impedance	13, 14		50		$\Omega$	
Prescaler input capacitance	13, 14		2		pF	
<b>SDA, SCL</b>						
Input high voltage	4, 5	3		5.5	V	Input voltage = $V_{CC}$ Input voltage = 0V When $V_{CC} = 0\text{V}$
Input low voltage	4, 5	0		1.5	V	
Input high current	4, 5			10	$\mu\text{A}$	
Input low current	4, 5			-10	$\mu\text{A}$	
Leakage current	4, 5			10	$\mu\text{A}$	
<b>SDA</b>						
Output voltage	4			0.4	V	$I_{sink} = 3\text{mA}$
Charge pump current low	1		$\pm 50$		$\mu\text{A}$	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		$\pm 170$		$\mu\text{A}$	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			$\pm 5$	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500			$\mu\text{A}$	$V_{pin\ 16} = 0.7\text{V}$
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	$\Omega$	
Crystal oscillator drive level	2		80		mVp-p	
Crystal oscillator negative resistance	2	750			$\Omega$	
<b>Output Ports</b>						
P0, P3 sink current	10, 11	0.7	1	1.5	mA	$V_{OUT} = 12\text{V}$
P0, P3 leakage current	10, 11			10	$\mu\text{A}$	$V_{OUT} = 13.2\text{V}$
P4-P7 sink current	9-6	10			mA	$V_{OUT} = 0.7\text{V}$
P4-P7 leakage current	9-6			10	$\mu\text{A}$	$V_{OUT} = 13.2\text{V}$
<b>Input Ports</b>						
P3 input current high	10			+10	$\mu\text{A}$	$V_{pin\ 10} = 13.2\text{V}$
P3 input current low	10			-10	$\mu\text{A}$	$V_{pin\ 10} = 0\text{V}$
P4,P5,P7 input voltage low	9,8,6			0.8	V	
P4,P5,P7 input voltage high	9,8,6	2.7			V	
P6 input current high	7			+10	$\mu\text{A}$	See Table 3 for ADC Levels
P6 input current low	7			-10	$\mu\text{A}$	



# SP5055

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

## APPLICATION

A typical Application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

	MSB					LSB				
<b>Address</b>	1	1	0	0	0	MA1	MA0	0	A	<b>Byte 1</b>
<b>Programmable divider</b>	0	2 <sup>14</sup>	2 <sup>13</sup>	2 <sup>12</sup>	2 <sup>11</sup>	2 <sup>10</sup>	2 <sup>9</sup>	2 <sup>8</sup>	A	<b>Byte 2</b>
<b>Programmable divider</b>	2 <sup>7</sup>	2 <sup>6</sup>	2 <sup>5</sup>	2 <sup>4</sup>	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	A	<b>Byte 3</b>
<b>Charge pump and test bits</b>	1	CP	T1	T0	1	1	1	OS	A	<b>Byte 4</b>
<b>I/O port control bits</b>	P7	P6	P5	P4	P3	X	X	P0	A	<b>Byte 5</b>

Table 1 Write data format (MSB transmitted first)

<b>Address</b>	1	1	0	0	0	MA1	MA0	1	A	<b>Byte 1</b>
<b>Status byte</b>	POR	FL	I2	I1	I0	A2	A1	A0	A	<b>Byte 2</b>

Table 2 Read data format (MSB is transmitted first)

- A** : Acknowledge bit
- MA1, MA0** : Variable address bits (see Table 4)
- CP** : Charge Pump current select
- T1** : Test mode selection
- T0** : Charge pump disable
- OS** : Varactor drive Output disable Switch
- P7, P6, P5, P4, P3, P0** : Control output states
- POR** : Power On Reset indicator
- FL** : Phase lock detect flag
- I2, I1, I0** : Digital information from Ports P7, P5 and P4, respectively
- A2, A1, A0** : 5 Level ADC data from P6 (see Table 3)
- X** : Don't care

A2	A1	A0	Voltage input to P6
1	0	0	0.6V <sub>CC</sub> to 13.2V
0	1	1	0.45V <sub>CC</sub> to 0.6V <sub>CC</sub>
0	1	0	0.3V <sub>CC</sub> to 0.45V <sub>CC</sub>
0	0	1	0.15V <sub>CC</sub> to 0.3V <sub>CC</sub>
0	0	0	0 to 0.15V <sub>CC</sub>

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to 0.2V <sub>CC</sub>
0	1	Always valid
1	0	0.3V <sub>CC</sub> to 0.7V <sub>CC</sub>
1	1	0.8V <sub>CC</sub> -13.2V

Table 4 Address selection

Fig. 3 Data formats

**APPLICATION**

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

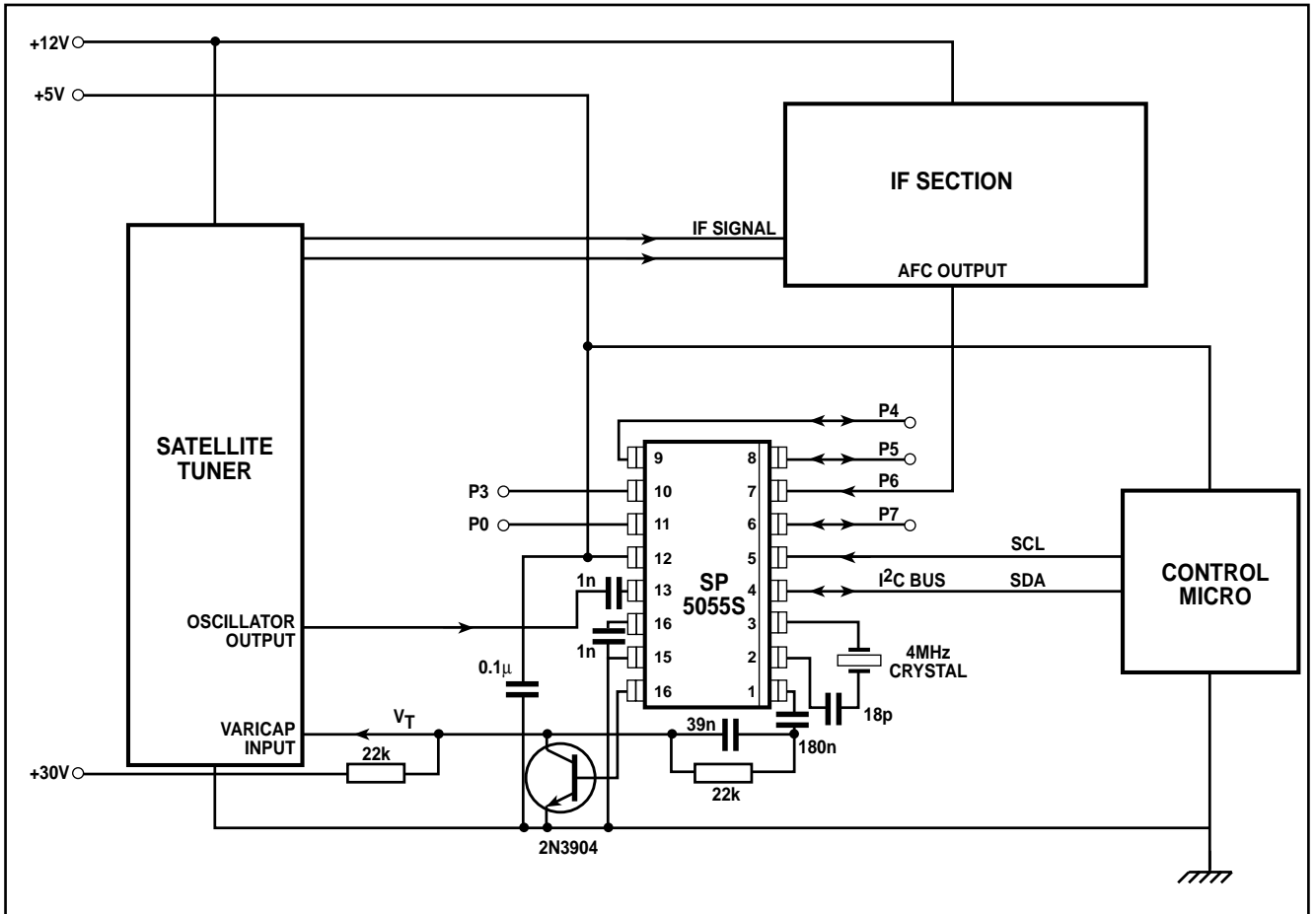


Fig. 4 Typical application

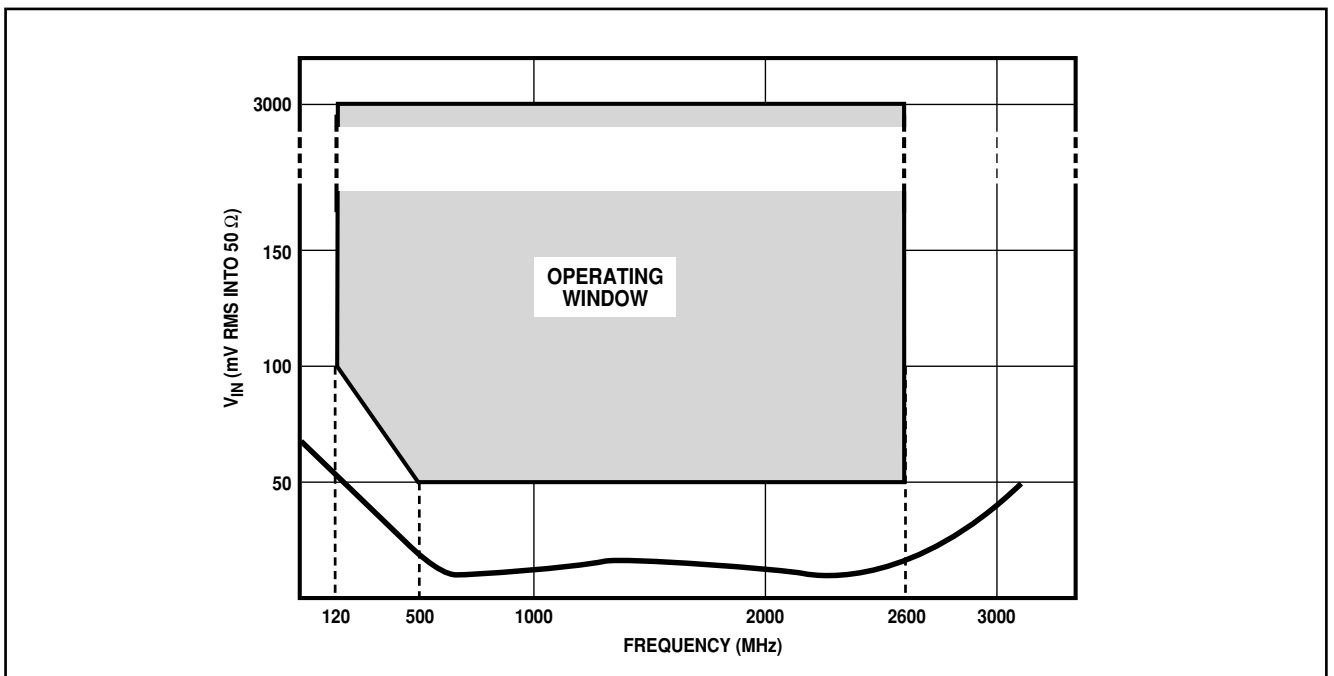


Fig. 5 Typical input sensitivity

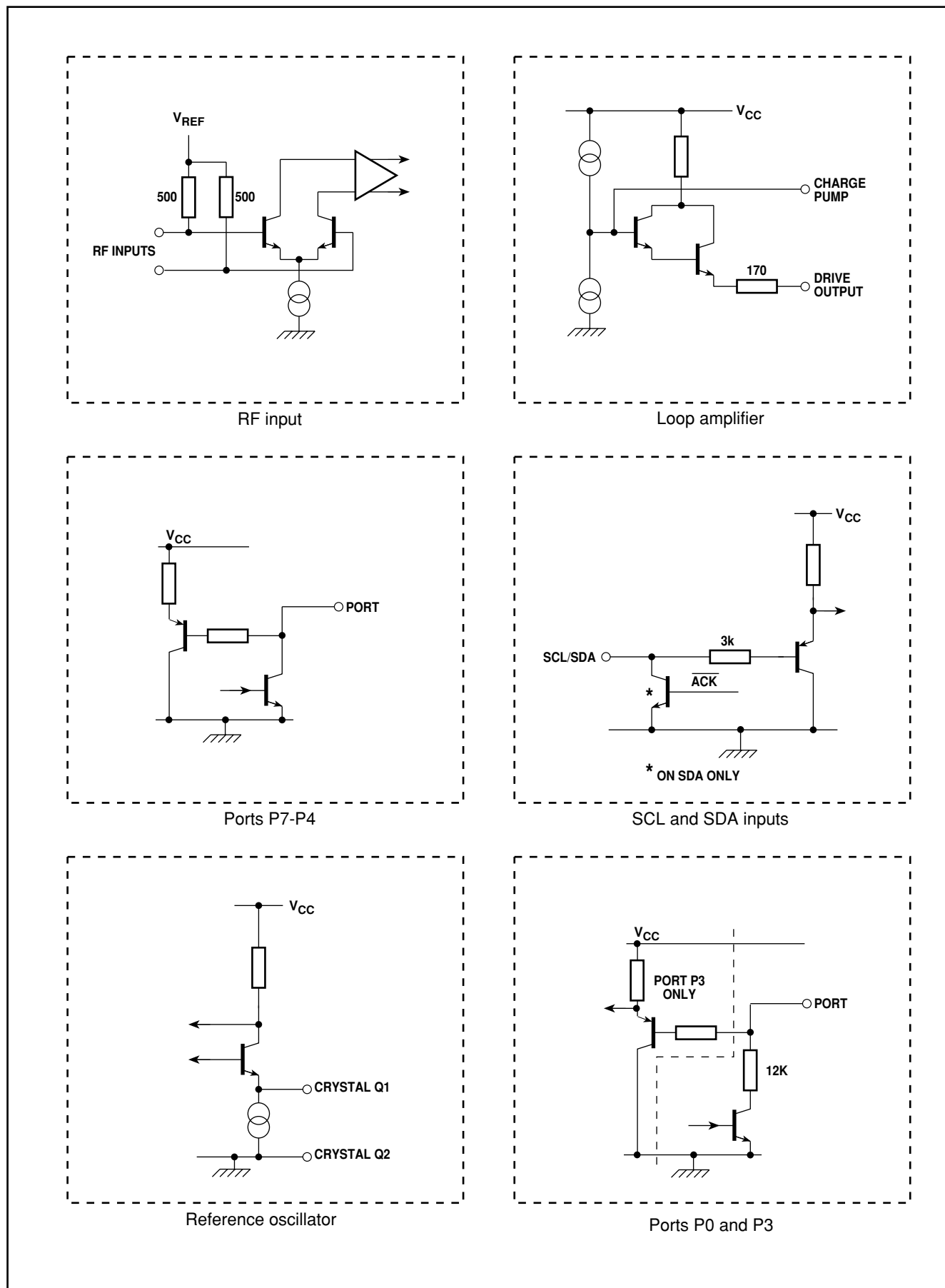


Fig. 6 SP5055 Input/output interface circuits

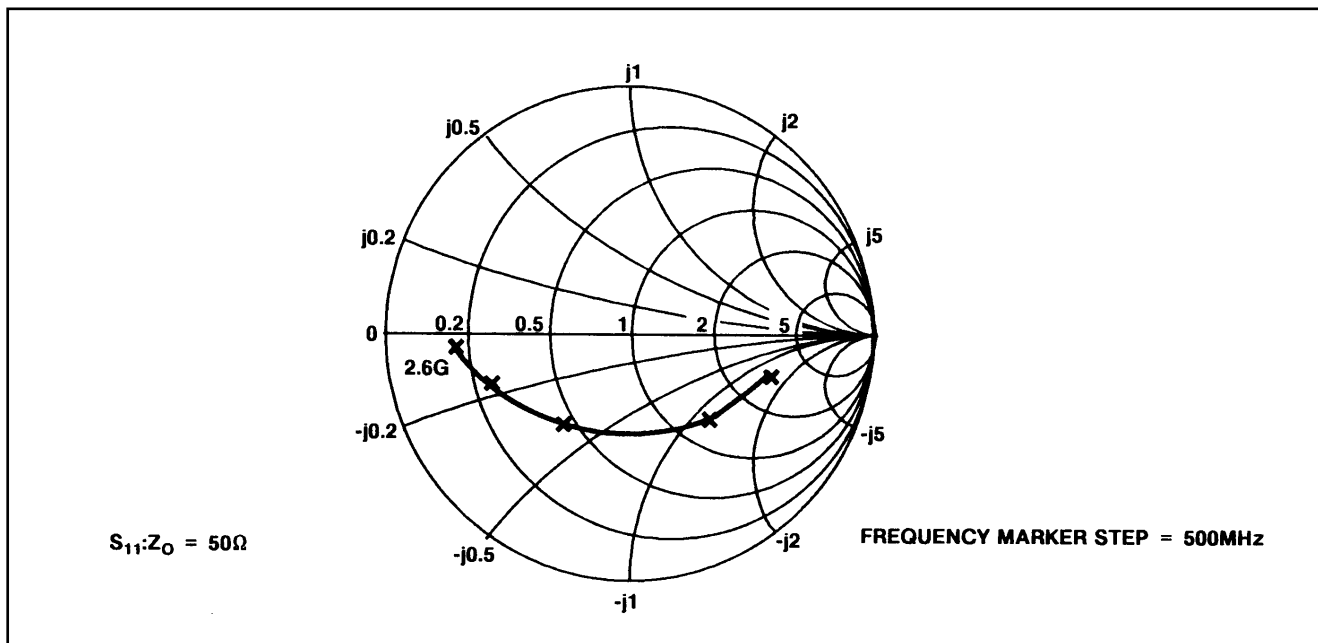
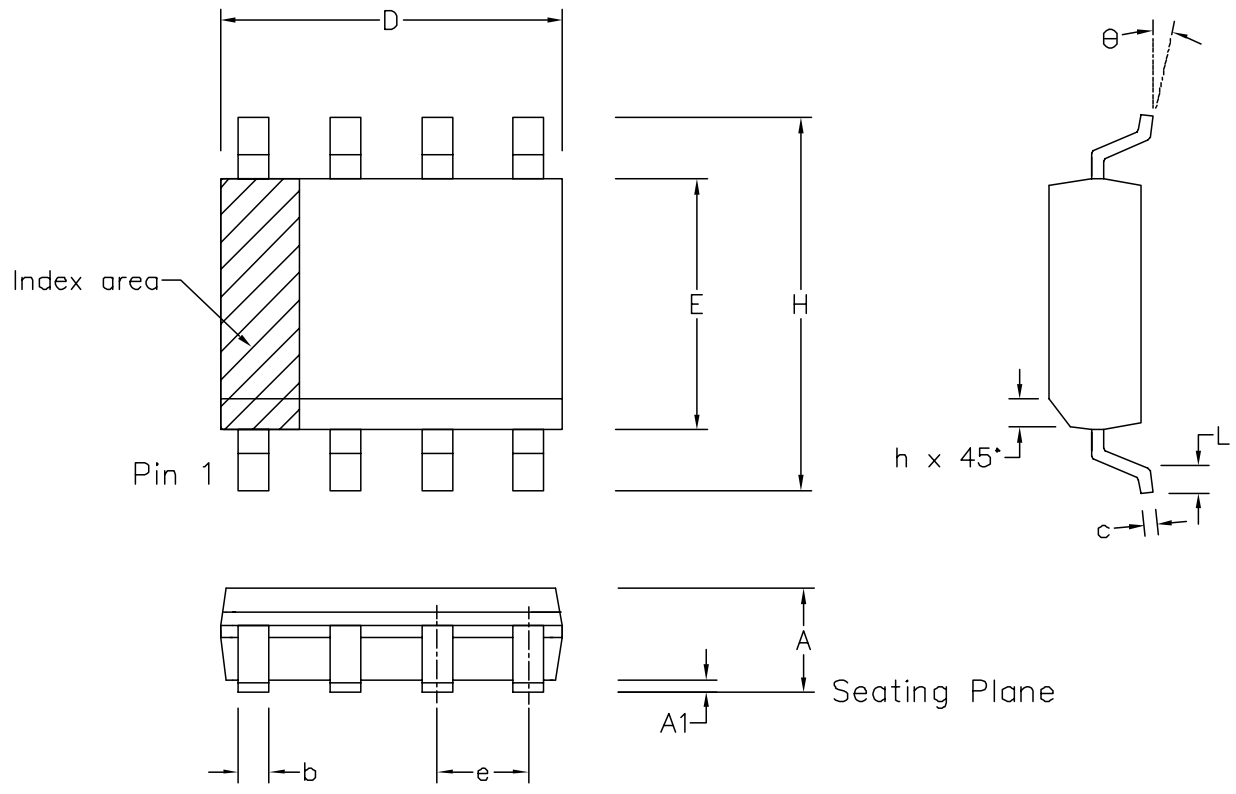


Fig. 7 Typical input impedance

**ABSOLUTE MAXIMUM RATINGS**

All voltages are referred to  $V_{EE}$  and pin 3 at 0V

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	-0.3	7	V	
RF input voltage	13, 14		2.5	Vp-p	
Port voltage	6-11	-0.3	14	V	Port in off state
	6-9	-0.3	6	V	Port in on state
	10, 11	-0.3	14	V	Port in on state
Total port output current	6-11		50	mA	
RF input DC offset	13, 14	-0.3	$V_{CC}+0.3$	V	
Charge pump DC offset	1	-0.3	$V_{CC}+0.3$	V	
Drive DC offset	16	-0.3	$V_{CC}+0.3$	V	
Crystal oscillator DC offset	2	-0.3	$V_{CC}+0.3$	V	
SDA, SCL input voltage	4, 5	-0.3	$V_{CC}+0.3$	V	With $V_{CC}$ applied $V_{CC}$ not applied
		-0.3	5.5	V	
Storage temperature		-55	+125	°C	
Junction temperature			+150	°C	
MP 16 Thermal resistance, chip-to-ambient			111	°C/W	
MP 16 Thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5.5V			440	mW	All ports off



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
O	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:

1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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APPROVED					

ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for 16 lds SOIC(N)-0.150" Body Width (MP)

Drawing Number  
GPD00012





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